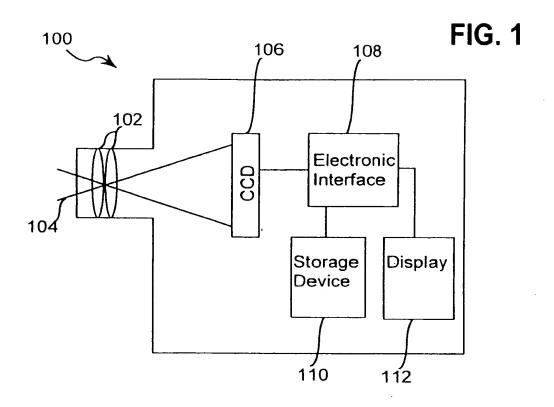
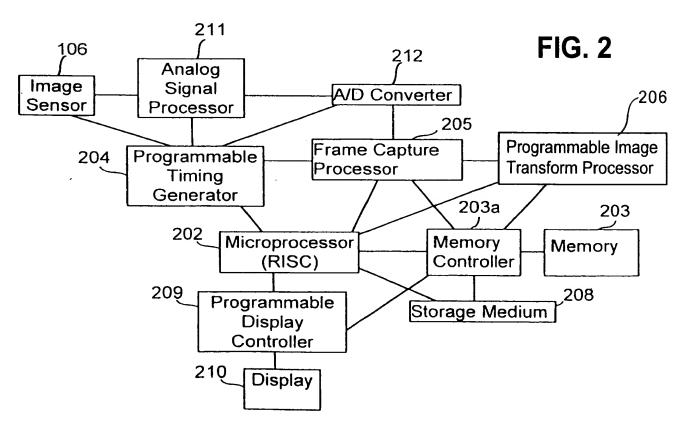
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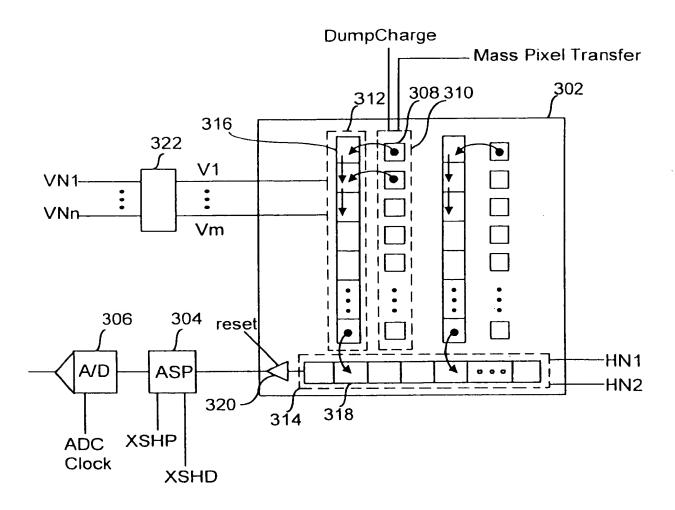
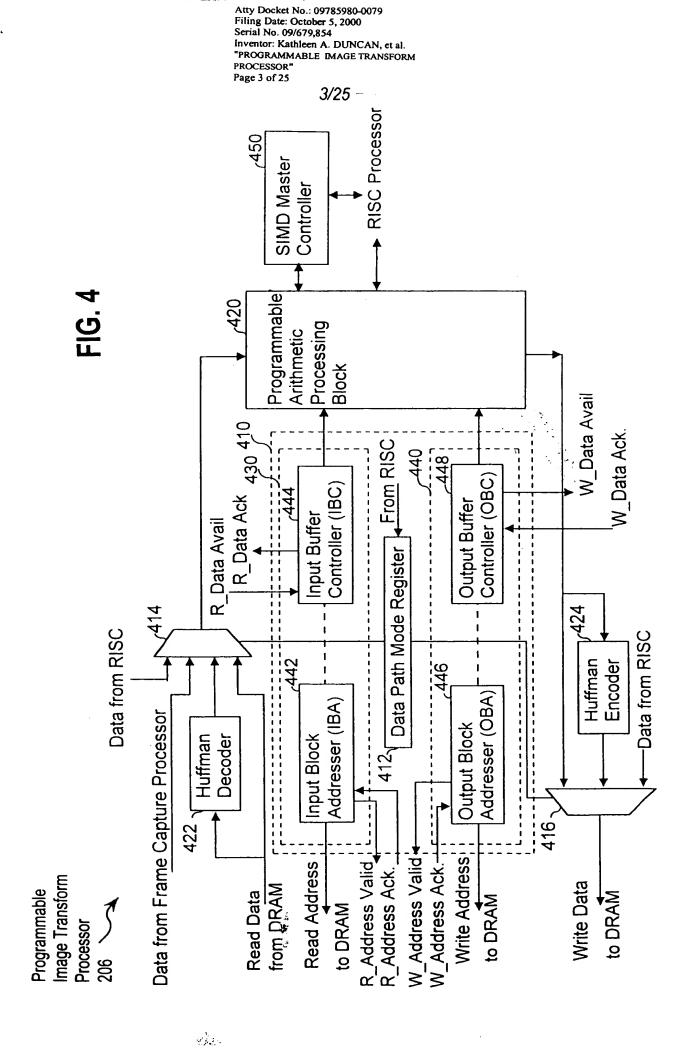


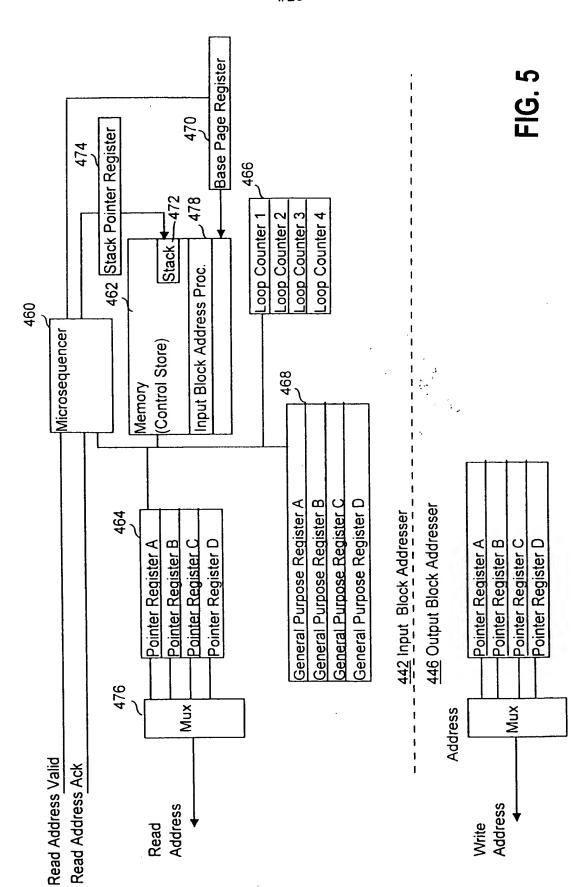
FIG. 3

1.0



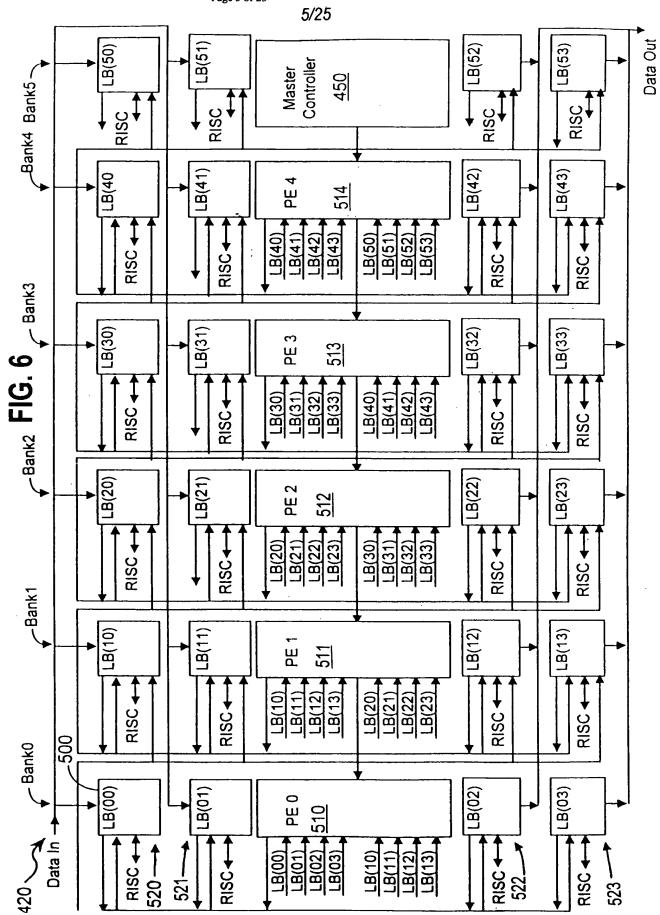
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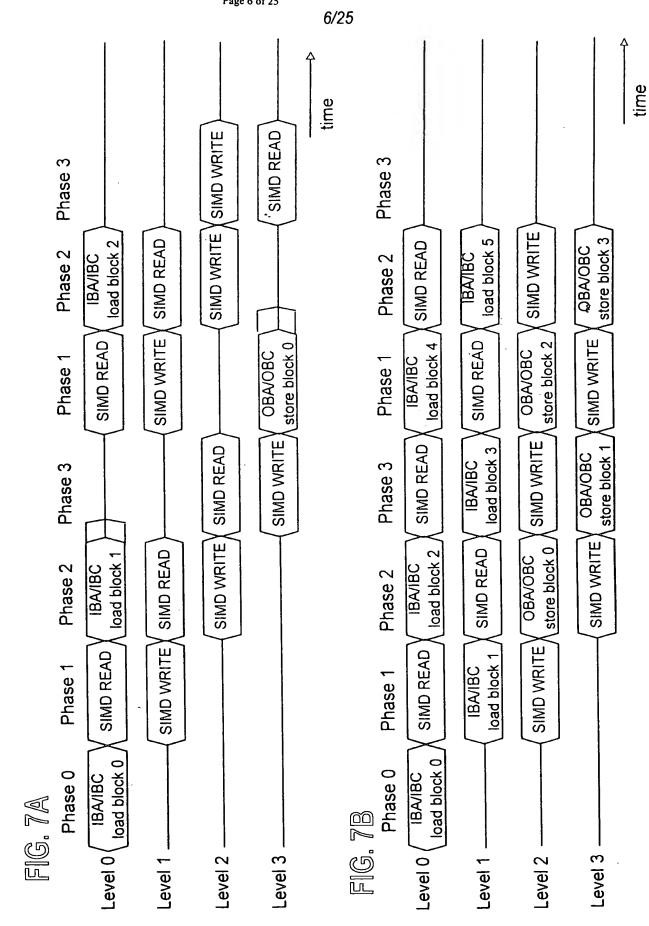


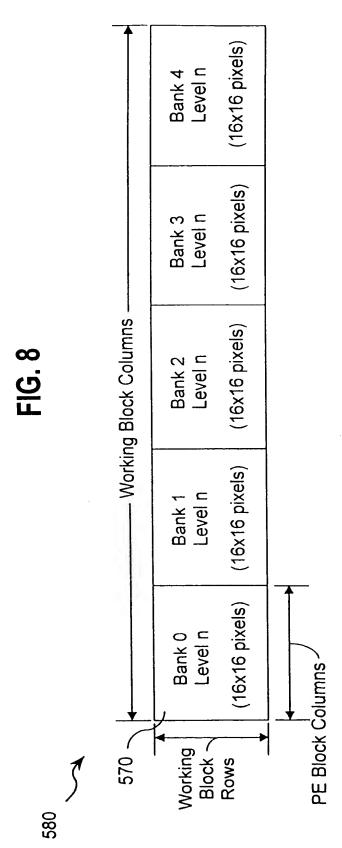
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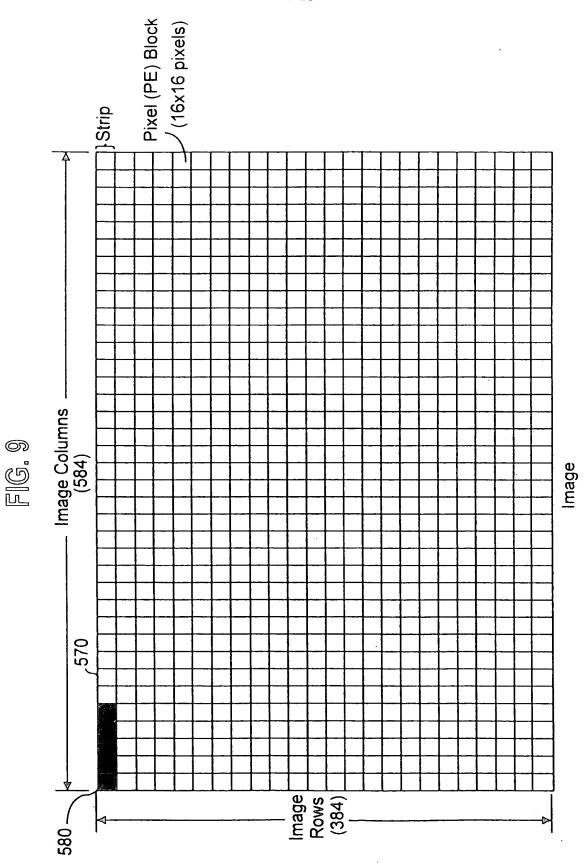
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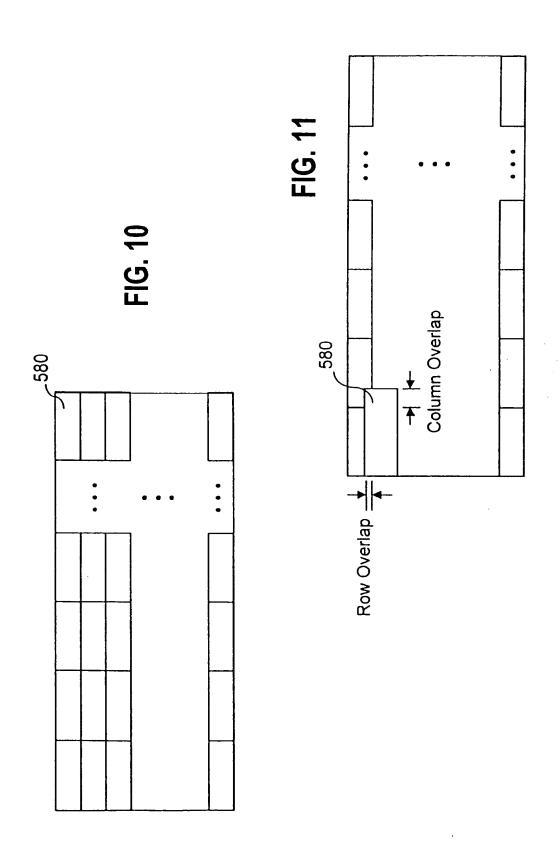
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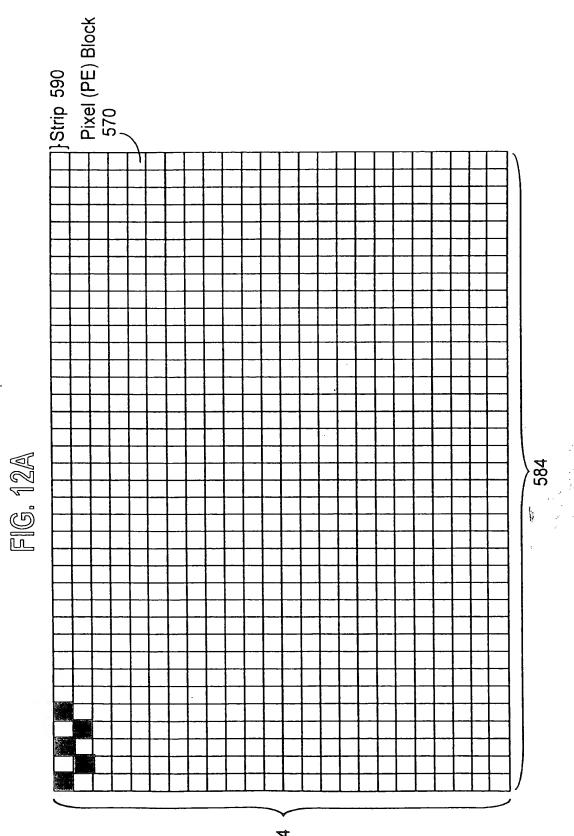
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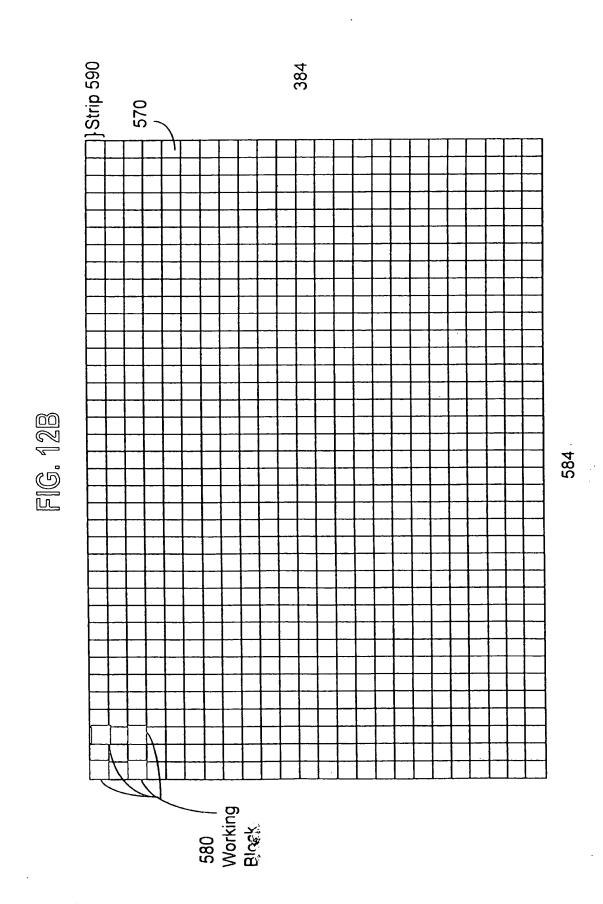
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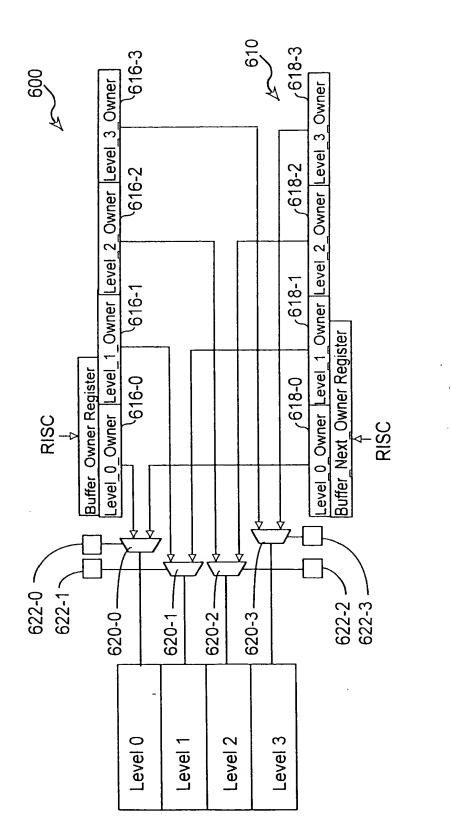
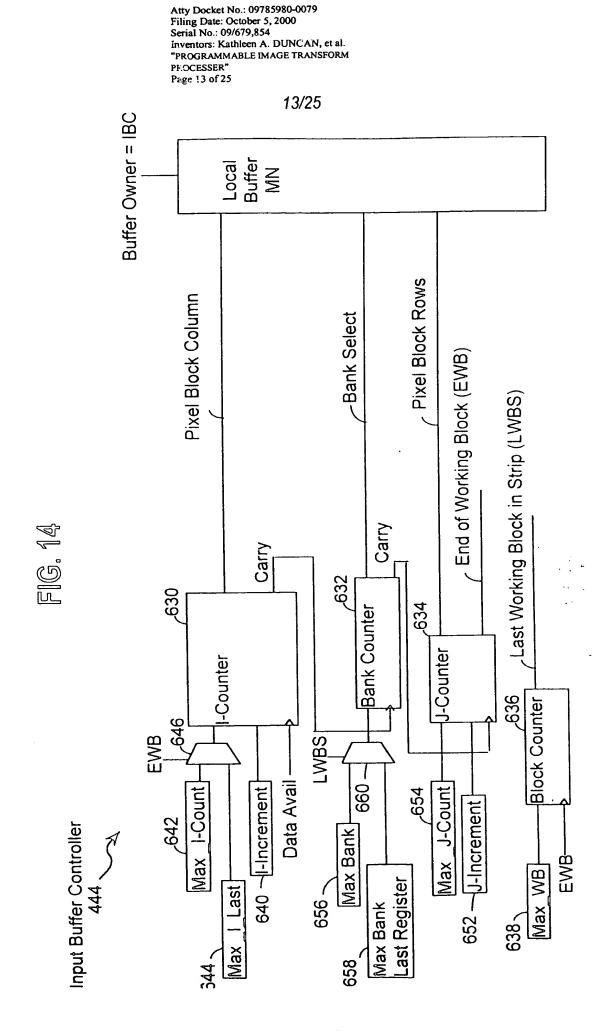


FIG. 13



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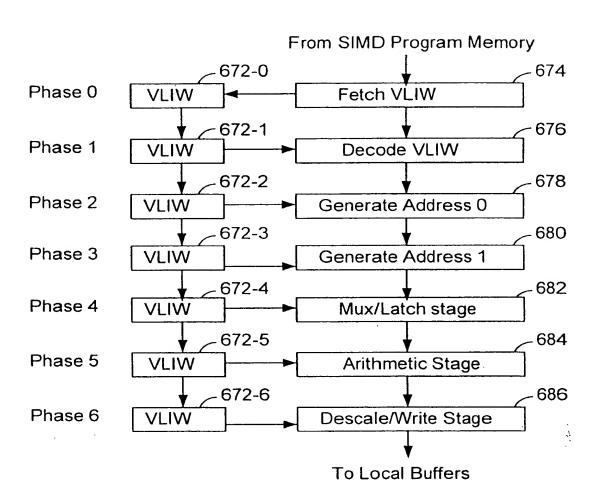


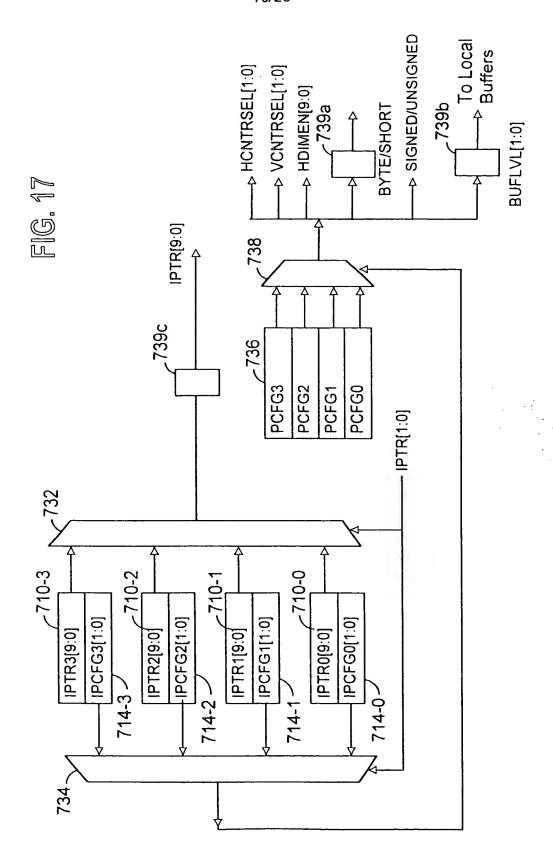
FIG. 15

*PROGRAMMABLE IMAGE TRANSFORM PROCESSOR" Page 15 of 25 15/25 To RISC TPC Halt Bit PE Enable Bits Instruction Pointer 692 Image Processing Procedure 722 .698 702 SIMD Program Memory 724 Coefficient Storage Data Port Program Storage Data Port 726 969 694 Interrupt Status Register Interrupt Mask Register Port Coefficient Address Data Memory CSR Register 9 **Processing Unit** Controller Master SIMD Configuration Regs Configuration Regs and Coefficients Control Signals to Processing Elements Counter 0 Byte Address Input Pointers 714 Input Ptr. 716 Input Ptr Local Buffer Pointers 712 \Output Counter 708 Stack

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"PROGRAMMABLE IMAGE TRANSFORM PROCESSOR" Page 17 of 25 17/25 To pointer register To Local Buffer \ BYTE/SHORT 768 764 7 99/ 4 1/0 IPTR[9:0] 760 Selection Signal 759b 759a 758 Out-of-bounds 752 750 HDIMEN[9:0] 222 × + 748 HDIMEN[9:0] _ HDIMEN[9:0] — 969 754 HOFF[3:0] __ VCNTRSEL[1:0] HCNTRSEL[1:0] 755 4 744 VOFF[3:0] _ 746 CTR3 CTR2 CTR0 CTR1

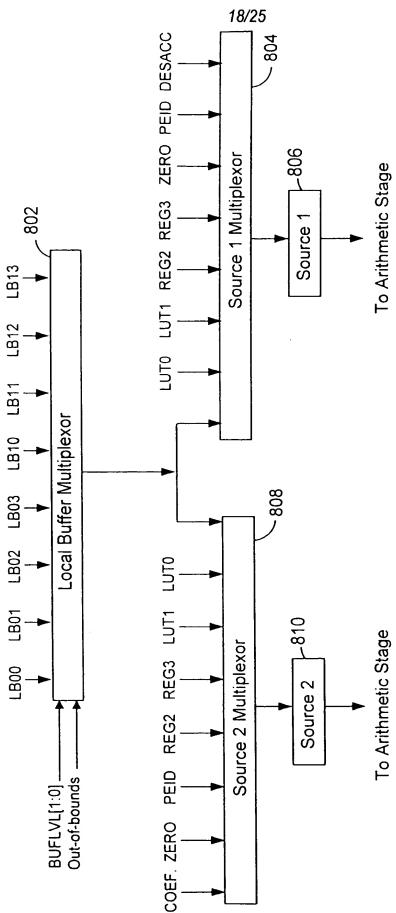
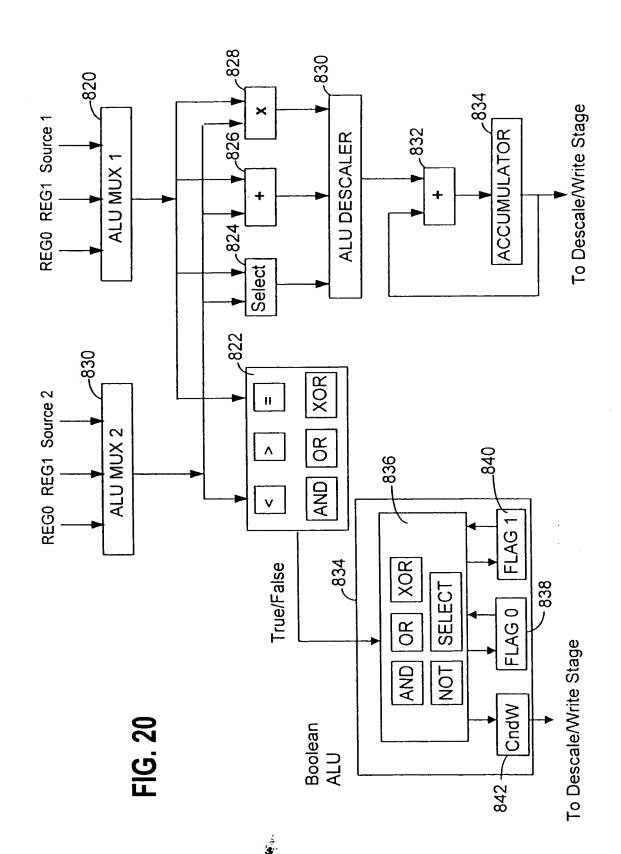


FIG 19

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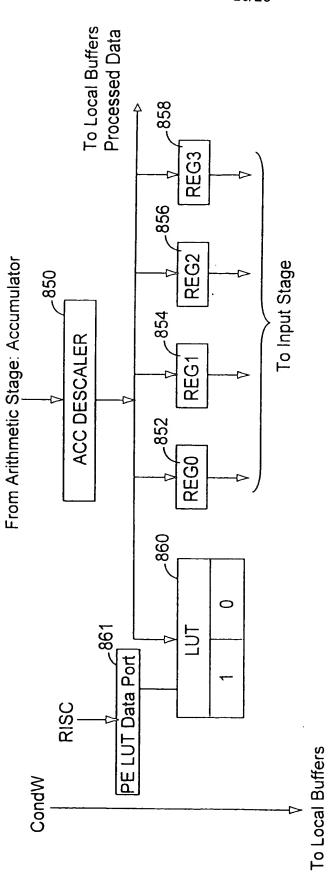
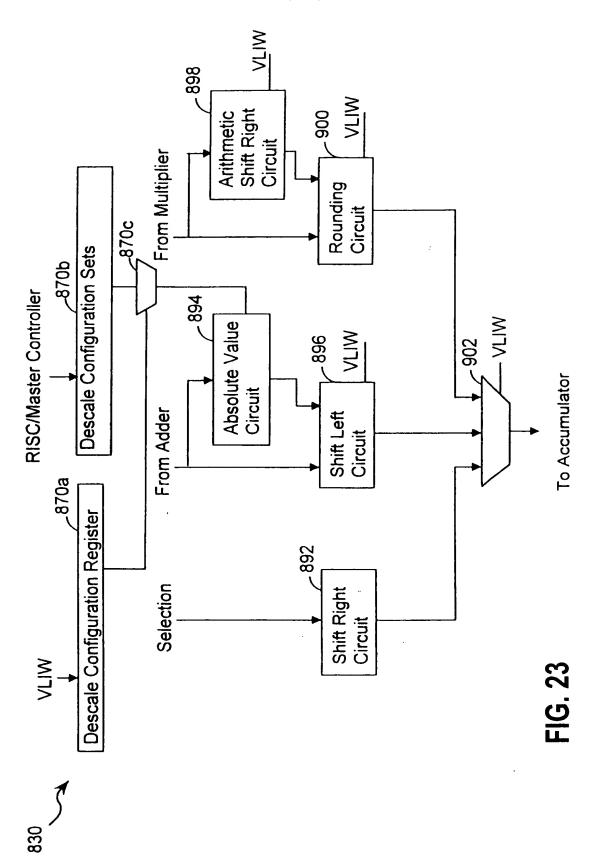


FIG. 24

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Page 21 of 25 21/25 RISC 7 886 Upper Bound Descale Register 878 Absolute Value Circuit -882 876 -874 To Summing Circuit From Accumulator Rounding Circuit Shifter Descale Configuration Register 890 880 884 Lower Bound Descale Register Absolute Value Saturation Selection 850 RISC/Master Controller -870b Round RISC -870c Shift Configuration Sets Descale

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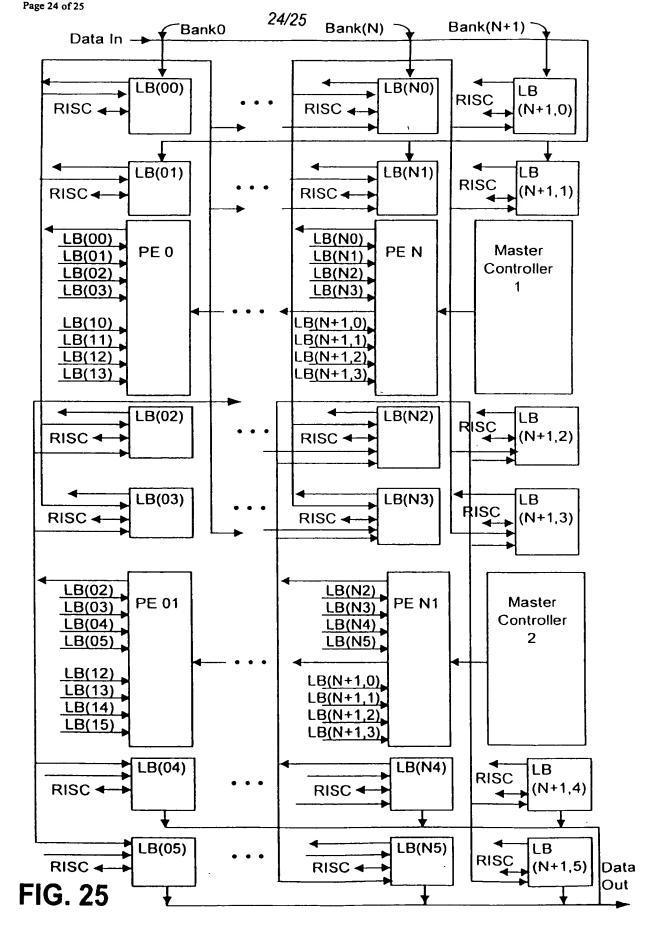


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"PROGRAMMABLE IMAGE TRANSFORM PROCESSOR* Page 23 of 25 23/25 (N+1,3)Data Out (N+1,0) Master Controller (N+1) (N+1) В 9 a Bank(N+1) RISC + RISC RISC RISC LB(N2) **LB(N3)** LB(N0) LB(N1) PE N Bank(N) LB(53) LB(52) LB(41) B(42) LB(51) LB(40) LB(43) LB(50) RISC RISC RISC RISC Bank₂ LB(22) LB(23) LB(20) LB(21) PE 2 B(33) LB(21) LB(23) LB(30) B(31) LB(32) LB(22) RISC RISC RISC RISC Bank1 LB(10) LB(12) LB(13) LB(11) Ы RISC + LB(10) LB(12) B(21) .B(22) _B(11) LB(13) B(20) .B(23) RISC. RISC. RISC LB(01) LB(03) LB(00) LB(02) PE 0 FIG. 24 Data In 🚽 LB(12) LB(00) LB(01) B(02) LB(03) B(10) LB(11) RISC. RISC. RISG RISC

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